Claims

What is claimed is:

1. A processor comprising:

first classification circuitry;

first memory circuitry coupled to the first classification circuitry, the first memory circuitry being configurable to store at least a portion of a given packet to be processed by the first classification circuitry;

second classification circuitry; and

second memory circuitry coupled to the second classification circuitry, the second memory circuitry being configurable to store at least a portion of the given packet to permit processing thereof by the second classification circuitry;

wherein the first classification circuitry is operative to perform a first pass classification on the given packet, and further wherein the portion of the given packet storable in the second memory circuitry comprises a portion of the given packet determined by the first pass classification to be required for a second pass classification performed by the second classification circuitry.

2. The processor of claim 1 wherein the processor is configured to provide an interface between a network from which the packet is received and a switch fabric.

3. The processor of claim 1 wherein the portion of the given packet storable in the second memory circuitry comprises at least a payload portion of the packet from which at least one of a header and a trailer have been removed.

4. The processor of claim 1 wherein the portion of the given packet storable in the second memory circuitry comprises at least a portion of the packet from which information added to the packet in an associated traffic management process has been removed.

5. The processor of claim 1 wherein the first memory circuitry comprises a first internal memory of the processor coupled to the first classification circuitry via a first memory controller.

6. The processor of claim 1 wherein the second memory circuitry comprises an internal buffer memory of the processor coupled to the second classification circuitry via a second memory controller.

7. The processor of claim 1 wherein the first memory circuitry and the second memory circuitry comprise different portions of a single memory internal to the processor.

8. The processor of claim 1 wherein the second memory circuitry has a larger storage capacity than the first memory circuitry.

9. The processor of claim 1 wherein the first pass classification is configured to perform at least a portion of a reassembly operation for the given packet, such that a portion of the packet required for performing the reassembly operation need not be stored in the second memory circuitry.

10. The processor of claim 1 wherein the first pass classification is configured to perform a parity check for the given packet, such that a portion of the packet required for performing the parity check need not be stored in the second memory circuitry.

11. The processor of claim 1 wherein the first pass classification comprises at least one of a reassembly operation, a parity check and a priority determination.

12. The processor of claim 1 wherein the first pass classification generates information which is passed in a specified data structure to the second classification circuitry for use in the second pass classification.

13. The processor of claim 1 wherein the first pass classification is performed on a plurality of cells comprising the given packet.

14. The processor of claim 1 wherein the portion of the given packet determined by the first pass classification is determined in accordance with one or more instructions provided to the processor under control of a host device operatively coupled to the processor.

15. The processor of claim 1 wherein the processor comprises a network processor.

16. The processor of claim 1 wherein the processor is configured as an integrated circuit.

17. A method for use in a processor comprising first and second classification circuitry coupled to respective first and second memory circuitry, the method comprising the steps of:

storing in the first memory circuitry at least a portion of a given packet to be processed by the first classification circuitry; and

performing in the first classification circuitry a first pass classification on the given packet, wherein a portion of the given packet storable in the second memory circuitry comprises a portion of the given packet determined by the first pass classification to be required for a second pass classification to be performed by the second classification circuitry.